REMARKS

Claims 1-2, 5-17, and 19-22 are pending in the application. Claims 3, 4, and 18 have been canceled. Of these, claims 1, 15, and 20 are independent. Favorable consideration and examination are respectfully requested.

Claims 1, 2, 5-8, 15-17, 20 and 21 were rejected in the parent case of this application under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,074,921 (Lin); claims 3, 9, 18, 19 were rejected under §103 over Lin; and claims 2 and 22 were rejected under §103 over Lin in view of U.S. Patent No. 6,080,655 (Givens). Applicants address these rejections here in order to advance prosecution.

Independent claim 1 defines a method of fabricating a semiconductor structure. The method includes selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, Lin teaches a process in which:

> "The polysilicon member has a thickness extending above the source and drain, and is bounded by a pair of spacer walls. The process also includes covering the source, the drain, the gate, and the spacer walls with a silicon nitride layer and depositing a silicon dioxide layer on the silicon nitride layer. At least a portion of the nitride layer and the silicon dioxide layer combine to provide a thickness greater than the thickness of the polysilicon member. During the process, a portion of the silicon dioxide layer is removed by chemical mechanical polishing to expose the polysilicon member without exposing the source or drain, and define a first generally planar surface. [Emphasis added]

As shown, for example, in FIG. 1e, Lin's process removes a portion of the polysilicon structure 43 and a portion of the sidewall spacers 37 to ensure a planar surface. Lin's process determines

the completion of the chemical mechanical polishing (CMP) etch based on the planarity of the structure, but does not disclose or suggest selecting the first chemical mechanical polishing rate (silicide polishing rate) to be higher than the second chemical mechanical polishing rate (polysilicon polishing rate) as in the applicant's claim 1. For at least the foregoing reasons, claim 1 is believed to be allowable.

Amended claim 20 includes features that are similar to those of claim 1. Claim 20 is believed to be allowable for at least the same reasons noted above with respect to claim 1.

Independent claim 15 defines a method of fabricating a semiconductor structure. The method includes forming a polysilicon feature on a semiconductor substrate having an intermediate gate dielectric layer, depositing a first metal layer over the polysilicon feature, reacting the first metal layer with the polysilicon feature to form a metal silicide, depositing a dielectric layer over the metal silicide and the semiconductor substrate, and removing a portion of the dielectric layer over the metal silicide to expose a portion of the metal silicide. The method also includes removing the portion of the metal silicide by chemical mechanical polishing, removing the polysilicon feature to create an opening in the gate dielectric layer, removing the gate dielectric layer, and oxidizing the semiconductor substrate to form a new gate dielectric layer.

The applied art is not understood to disclose or to suggest the foregoing features of claim 15. As described above, Lu is not understood to disclose or to suggest at least removing the polysilicon feature, removing the gate dielectric layer, and oxidizing the semiconductor substrate to form a new gate dielectric layer.

In Lin's processes, described in relation to FIGS. 1a-f, 3a-f, 4a-h, 5a-f, 6a-e, and 8a-e, a portion of the original polysilicon layer remains during the fabrication process. In an alternate embodiment shown in Lin's FIGS. 7a-c, the polysilicon layer is removed to form a void between the sidewall spacers. In this process, a portion of the gate oxide layer members 44, 54 may also be removed during the polysilicon etch. As a result, the gate oxide is surface cleaned and a controlled gate oxide regrowth is performed using conventional techniques" (col. 14, lines 59-63). Lin does not disclose or suggest "removing the intermediate dielectric layer, and oxidizing the semiconductor substrate to form a gate dielectric layer" as in the applicant's claim 1. For at least the foregoing reasons, claim 15 is believed to be allowable.

Applicants' attorney can be reached at the address shown below. Telephone calls regarding this application should be directed to 617-521-7896.

No fee is believed to be due for this Amendment; however, if any fees are due, please charge them to Deposit Account 06-1050.

Respectfully submitted,

Date: May 10, 2004

Paul A. Pysher
Reg. No. 40,780

Attorneys for Intel
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906
20841571.doc